NOC:VLSI Design Verification and test - Video course

COURSE OUTLINE

Digital VLSI Design flow comprises three basic phases: Design, Verification and Test. The web course would cover theoretical, implementation and CAD tools pertaining to these three phases. Although there can be individual full courses for each of these phases, the present course aims at covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow.

VLSI Design: High level Synthesis, Verilog RTL Design, Combinational and Sequential Synthesis Logic Synthesis (for large circuits).

Verification Techniques: Introduction to Hardware Verification and methodologies, Binary Decision Diagrams(BDDs) and algorithms over BDDs, Combinational equivalence checking, Temporal Logics, Modeling sequential systems and model checking, Symbolic model checking.

VLSI Testing: Introduction, Fault models, Fault Simulation, Test generation for combinational circuits, Test generation algorithms for sequential circuits and Built in Self test.

COURSE DETAIL

Sl.No	Topics
1.	**Design** **Module I: Introduction** Lecture I: Introduction to Digital VLSI Design Flow Lecture II: High Level Design Representation Lecture III: Transformations for High Level Synthesis
2.	**Module II: Scheduling, Allocation and Binding** Lecture I: Introduction to HLS: Scheduling, Allocation and Binding Problem Lecture II and III: Scheduling Algorithms

NP-TEL

NPTEL

http://nptel.ac.in

Electronics & Communication Engineering

Pre-requisites:

Digital Design

Coordinators:

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	Lecture IV: Binding and Allocation Algorithms
3.	**Module III: Logic Optimization and Synthesis** Lecture I,II and III: Two level Boolean Logic Synthesis Lecture IV: Heuristic Minimization of Two-Level Circuits Lecture V: Finite State Machine Synthesis Lecture VI: Multilevel Implementation
4.	**Verification** **Module - IV: Binary Decision Diagram** Lecture-I: Binary Decision Diagram: Introduction and construction Lecture-II: Ordered Binary Decision Diagram Lecture-III: Operations on Ordered Binary Decision Diagram Lecture-IV: Ordered Binary Decision Diagram for Sequential Circuits
5.	**Module - V: Temporal Logic** Lecture-I: Introduction and Basic Operations on Temporal Logic Lecture-II: Syntax and Semantics of CLT Lecture-III: Equivalence between CTL Formulas
6.	**Module-VI: Model Checking** Lecture-I: Verification Techniques Lecture-II, III and IV: Model Checking Algorithm Lecture-V: Symbolic Model Checking
7.	**Test** **Module VII: Introduction to Digital Testing** Lecture-I: Introduction to Digital VLSI Testing Lecture-II: Functional and Structural Testing Lecture-III: Fault Equivalence
8.	**Module VIII: Fault Simulation and Testability Measures** Lecture-I, II and III: Fault Simulation Lecture-IV: Testability Measures (SCOAP)
9.	**Module IX: Combinational Circuit Test Pattern Generation** Lecture-I: Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras

	Lecture-II and III: D-Algorithm
10.	**Module X: Sequential Circuit Testing and Scan Chains** Lecture-I: ATPG for Synchronous Sequential Circuits Lecture-II and III: Scan Chain based Sequential Circuit Testing
11.	**Module XI: Built in Self test (BIST)** Lecture I and II: Built in Self Test Lecture III and IV: Memory Testing

References:

1. D. D. Gajski, N. D., Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.
3. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
4. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004
5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000