

## PROF. PARASURAMAN SWAMINATHAN

Department of Metallurgy and Material Science IIT Madras

**INTENDED AUDIENCE :** Engineering and Science students at the UG and PG level

**INDUSTRIES APPLICABLE TO**: Semiconductor device fabrications companies such as TSMC and Applied Materials will value this course

## COURSE OUTLINE :

The course is intended to provide an understanding of current fabrication practices used in the semiconductor industry, along with the challenges and opportunities in Device Fabrication. It caters to UG and PG students from diverse backgrounds such as Chemical, Electrical, Mechanical, Metallurgy, Materials Science, Physics, and Chemistry. The course provides an overview on integrated circuit fabrication along with practices and challenges to continue to satisfy Moore's law.

## ABOUT INSTRUCTOR :

Prof. Parasuraman Swaminathan is a Professor in the Department of Metallurgical and Materials Engineering (MME), IIT Madras. He joined the institute in 2013. He has a B. Tech and M. Tech dual degree in MME from IIT Madras, and a PhD in Materials Science from the University of Illinois at Urbana-Champaign, USA. He then did a post doc in Johns Hopkins University and National Institute of Standards and Technology (NIST), USA on microelectronics device fabrication. He also worked in Intel Corp. for two years, primarily in their development fab facility. His research group is called the Electronic Materials and Thin Films group and they work in the area of printed electronics and thin film deposition. His research page can be accessed at https://mme.iitm.ac.in/swamnthn. Dr. Parasuraman has been offering this online course since 2016. He has published a textbook in this topic.

Link to the YouTube Channel: https://www.youtube.com/c/ElectronicMaterialsandThinFilmsLab

## COURSE PLAN :

- Week 1: Introduction and overview of semiconductor device fabrication
- Week 2: Fabrication operations: Oxidation, doping, and lithography
- Week 3: Fabrication processes: etching and growth. Process evaluation
- Week 4: Process yield, clean room design, and IC logic and packaging