MAPPING SIGNAL PROCESSING ALGORITHMS TO DSP ARCHITECTURES

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TYPE OF COURSE : New | Elective | UG/PG
COURSE DURATION : 12 weeks (29 Jul'19 - 18 Oct'19)
EXAM DATE : 16 Nov 2019

PRE-REQUISITES : - Digital Design fundamentals (UG) - Digital Signal Processing (UG) - Processor architecture (UG)

INTENDED AUDIENCE : Students interested in hardware (VLSI / FPGA) implementations of DSP systems; also useful for those using custom parallel architectures (GPU)

COURSE OUTLINE :
This course deals with the analysis of algorithms, and mapping them to architectures that are either custom designed or have specific extensions that make them better suited to certain kinds of operations. Topics covered include fundamental bounds on performance, mapping to dedicated and custom resource shared architectures, and techniques for automating the process of scheduling. Aspects of architectures such as memory access, shared buses, and memory mapped accelerators will be studied.

ABOUT INSTRUCTOR :
Prof. Nitin Chandrachoodan received his BTech (Electronics and Communication Engineering) from IIT Madras in 1996, and PhD from the University of Maryland at College Park in 2002, in the area of high-level synthesis techniques for mapping DSP algorithms to architectures. He has been with the Department of Electrical Engineering at IIT Madras since 2004, where he is currently an Associate Professor. His research interests include Digital Systems Design and Design Automation Tools and techniques, as well as Design of embedded systems with a special focus on assistive technologies. He has taught graduate courses on Digital Integrated Circuit Design and on mapping algorithms to architectures, and a UG course on data structures and algorithms, as well as a laboratory course on digital design using FPGAs. He is an Associate Editor of the Springer Journal of Signal Processing Systems.

COURSE PLAN :

Week 1: Review: Digital systems, DSP, computer architecture

Week 2: DSP system models; quality metrics and bounds; number representations

Week 3: DSP system models; quality metrics and bounds; number representations (contd)

Week 4: Implementation: dedicated hardware; transforms; resource sharing; Scheduling: time and resource bounds; allocation, binding, scheduling; techniques

Week 5: Implementation: dedicated hardware; transforms; resource sharing; Scheduling: time and resource bounds; allocation, binding, scheduling; techniques (contd)

Week 6: Implementation: dedicated hardware; transforms; resource sharing; Scheduling: time and resource bounds; allocation, binding, scheduling; techniques (contd)

Week 7: Architectures: programmable systems; FSMs and microprograms; instruction extensions; peripheral accelerators

Week 8: Architectures: programmable systems; FSMs and microprograms; instruction extensions; peripheral accelerators (contd)

Week 9: Architectures: programmable systems; FSMs and microprograms; instruction extensions; peripheral accelerators (contd)

Week 10: Memory and communication systems: bus structures; DMA; networks-on-chip

Week 11: Memory and communication systems: bus structures; DMA; networks-on-chip (contd)

Week 12: Specialized architectures: Systolic arrays; CORDIC; GPU