Optimization Techniques for Digital VLSI Design

Computer Science and Engineering

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About Instructor: Dr. Santosh Biswas is an Associate Professor in the Dept. of CSE IIT Guwahati. He has an experience of 8 years in teaching. His research interests are Fault Tolerance, VLSI Testing, Embedded Systems

Pre Requisites: : Basic knowledge of electronic design automation (EDA), digital design
Core/Elective: : Elective
UG/PG: : Both
Industry Support : Synopsys, Cadence, Mentor Graphics, Intel, Samsung, etc.

Course Intro: : Digital VLSI Design flow comprises three basic phases: Design, Verification and Test. This course will give a brief overview of the VLSI design flow. The primary emphasis of the course is to introduce the important optimization techniques applied in the Industry level electronic design automation (EDA) tools in the VLSI design flow. This course is unique in the sense that it will give a comprehensive idea about the widely used optimization techniques and their impact the generated hardware. The outline of the course is as follows: VLSI Design: Overview of digital VLSI design flow; High-level Synthesis, logic synthesis and physical synthesis and optimization techniques applied in these three steps; Impact of compiler optimization on hardware synthesis, 2-level logic optimization, multi-level logic optimizations, ESPRESSO; Technology Mapping: DSP and RAM inference for FPGA. RTL Optimizations: Area, power and timing optimization techniques like retiming, register balancing, folding. pipelining, and clock gating. VLSI Test: Introduction to Automatic Test Pattern Generation (ATPG), optimization Techniques for ATPG, design for Testability, optimization Techniques for design for testability, High-level fault modeling, RTL level Testing Verification: LTL and CTL based hardware verification, verification of large systems, binary decision diagram (BDD) based verification, arithmetic decision diagram based (ADD) and high-level decision diagram (HDD) based verification, symbolic model checking, bounded model checking.

COURSE PLAN

SL.NO	Week	Module Name
1	1	Introduction to Digital VLSI Design Flow
2	1	High-level Synthesis (HLS)
3	1	Impact of Compiler Optimizations on HLS
4	2	Heuristic based Optimization Techniques for HLS
5	3	Heuristic based logic optimization: EXPRESSO
6	4	Retiming for Clock period minimization
7	5	Introduction to Digital VLSI Testing, Automatic Test Pattern Generation (ATPG), Design for Testability
8	6	Optimization Techniques for Design for Testability
9	7	LTLCTL based Verification

10	8	ADD based verification, HDD based verification