

Computer Organization and Architecture

Type of Course : New

Course Snapshot : Core / UG, PG

: B.E/B.Tech, M.E/M.Tech, M.S

Pre-requisites Basic Programming, Digital Electronics

Course Duration : 30 hours / 12 weeks

Industry Support : All high end and embedded processors

related companies like Intel, AMD, Qualcomm,NVIDIA, IBM, Samsung, Motorola, Hewlett-Packard etc.

COURSE OUTLINE:

Computer Architecture talks about the basic digital hardware with which the processor is built and Computer Organization talks about the basic interface the digital hardware gives to the compiler and the operating systems to support the user demands. Study of Application Binary Interface is the subject matter of Computer Organization. How these functionalities are actually implemented is the subject matter of Computer Architecture. This course not only addresses the how and what but also the whys of Computer Architecture and Organization.

INSTRUCTOR:

Prof. V. Kamakoti Department of Computer Science and Engineering, IIT Madras

ABOUT INSTRUCTOR:

Prof. V. Kamakoti, Department of Computer Science and Engineering, IIT Madras specializes in the area of Computer Architecture and Secure Hardware Design. He is an advisor for many security critical organizations including Banking Institutions. He completed his Master of Science (By research) and PhD at the Department of Computer Science and Engineering, IIT Madras in the years 1992 and 1995 respectively. He completed his BE in Computer Science and Engineering from Sri Venketaswara College of Engineering (Affiliated to University of Madras) in the year 1989. He is a coordinator of the Information Security Education and Awareness program of the Department of Information Technology, Government of India

COURSE PLAN:

- High-Performance Circuit Design Fast Adder Circuits, Fast Multiplier Circuit Floating Point -Precision and Accuracy, Addition, Subtraction and Multiplication
- Programming using X86 Instruction Set Architecture Orthogonal ISA, C Constructs Mapping, Addressing Modes - Atomic and Predicated Instructions - General Purpose Registers -Expanding Opcodes
- 3. Pipelining Data Hazards Instruction Scheduling: Static and Dynamic Control Hazard, Branch Prediction
- 4. Segmentation Interrupts & Process Management- Paging Multitasking Virtual memory Task Switching
- Caches Shared Memory Architecture Mutual Exclusion Optimality of Parallel Algorithms -Current Trends in Computer Architecture