SWITCHING CIRCUITS AND LOGIC DESIGN

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INTENDED AUDIENCE : Any Engineering Students/Faculty
PRE-REQUISITES : Basic knowledge of electronics and electrical circuits
INDUSTRIES APPLICABLE TO : TCS, Wipro, CTS, Google, Microsoft, HP, Intel, IBM

COURSE OUTLINE :

This course will discuss the basic background of switching circuits, and discuss techniques for mapping the theory to actual hardware circuits. Synthesis and minimization techniques of combinational and sequential circuits shall be discussed in detail. Designing circuits using high-level functional blocks shall also be discussed. The course will closely follow the undergraduate curriculum existing in most engineering colleges.

ABOUT INSTRUCTOR :

Prof. Indranil Sengupta has obtained his B.Tech., M.Tech. and Ph.D. degrees in Computer Science and Engineering (CSE) from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of CSE, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences.

COURSE PLAN :

Week 01 : Introduction to number systems and codes, error detection and correction, binary arithmetic.
Week 02 : Switching primitives and logic gates, logic families: TTL, CMOS, memristors, all-optical realizations.
Week 03 : Boolean algebra: Boolean operations and functions, algebraic manipulation, minterms and maxterms, sum-of-products and product-of-sum representations, functional completeness.
Week 04 : Minimization of Boolean functions: K-map method, prime implicants, don't care conditions, Quine-McCluskey method, multi-level minimization.
Week 05 : Design of combinational logic circuits: adders and subtractors, comparator, multiplexer, demultiplexer, encoder, etc.
Week 06 : Representation of Boolean functions: binary decision diagram, Shannon's decomposition, Reed-Muller canonical form, etc.
Week 07 : Design of latches and flip-flops: SR, D, JK, T. Master-slave and edge-triggered flip-flops. Clocking and timing issues.
Week 08 : Synthesis of synchronous sequential circuits, Mealy and Moore machines, state minimization.
Week 09 : Design of registers, shift registers, ring counters, binary and BCD counters. General counter design methodology.
Week 10 : Algorithmic state machine and data/control path design.
Week 11 : Asynchronous sequential circuits: analysis and synthesis, minimization, static and dynamic hazards.
Week 12 : Testing and fault diagnosis in digital circuits: fault modeling, test generation and fault simulation, fault diagnosis, design for testability and built-in self-test.