HARDWARE MODELING USING VERILOG

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INTENDED AUDIENCE: Computer Science and Engineering ; Electronics and Communication Engineering ; Electrical Engineering

PRE-REQUISITES : Basic concepts in digital circuit design ; Familiarity with a programming language like C or C++

INDUSTRY SUPPORT : Intel, Cadence, Mentor Graphics, Synopsys, Xilinx.

COURSE OUTLINE:

The course will introduce the participants to the Verilog hardware description language. It will help them to learn various digital circuit modeling issues using Verilog, writing test benches, and some case studies.

ABOUT INSTRUCTOR:

Prof.Indranil Sengupta has obtained his B.Tech., M.Tech. and Ph.D. degrees in Computer Science and Engineering from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of Computer Science and Engineering, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences. His research interests include cryptography and network security, VLSI design and testing, and mobile computing.

He is a Senior Member of IEEE. He had been the General Chairs of Asian Test Symposium (ATS-2005), International Conference on Cryptology in India (INDOCRYPT-2008), International Symposium on VLSI Design and Test (VDAT-2012), International Symposium on Electronic System Design (ISED-2012), and the upcoming Conference on reversible Computation (RC-2017). He had delivered invited and tutorial talks in several conferences in the areas of VLSI design and testing, and network security.

COURSE PLAN:

Week 1: Introduction to digital circuit design flow (3 hours)

Week 2: Verilog variables, operators and language constructs (2 hours)

Week 3: Modeling combinational circuits using Verilog (2 hours)

Week 4: Modeling sequential circuits using Verilog (3 hours)

Week 5: Verilog test benches and design simulation (2 hours)

Week 6: Behavioral versus structural design modeling (2 hours)

Week 7: Miscellaneous modeling issues: pipelining, memory, etc. (2 hours)

Week 8: Processor design using Verilog (4 hours)