ADVANCED COMPUTER ARCHITECTURE

PROF.JOHN JOSE
Department of Computer Science and Engineering
IIT Guwahati

TYPE OF COURSE : Rerun | Elective | PG
COURSE DURATION : 8 weeks (21 Feb'22 - 15 Apr'22)
EXAM DATE : 24 Apr 2022

PRE-REQUISITES : A basic understanding of Computer Organisation & Architecture or Microprocessors

INTENDED AUDIENCE : Anyone in CSE and related fields (like ECE, EEE, IT etc.) with an interest of exploring Computer Architecture

INDUSTRIES APPLICABLE TO : Intel, AMD, IBM, Nvidia etc

COURSE OUTLINE :
Applications and handheld devices play a major role in ensuring comfort in our day- today life. These applications run on handheld electronic gadgets with high-end microprocessor support. Modern CPU designers handle challenges imposed by these applications with cost effective architectural enhancements. This course provides a deeper insight into the design of high-end microprocessors that will support the future applications.

ABOUT INSTRUCTOR :
Prof. John Jose is an Assistant Professor in Department of Computer Science and Engineering, Indian Institute of Technology, Guwahati. Prior to this he worked as faculty in Rajagiri School of Engineering and Technology and Viswajyothi College of Engineering and Technology, Kerala for 7 years. He completed his Ph.D degree in Department of Computer Science and Engineering, Indian Institute of Technology, Madras. He has guided over 8 M.Tech thesis and is currently supervising 6 PhD thesis and 2 M.Tech thesis. His area of interest is in on-chip interconnection networks and cache management techniques for large multicore systems. He is the principal investigator of two sponsored R&D projects funded by DST, Govt of India. He is having active research collaboration with University of Catania-Italy, ITRI Taiwan, and BITS Pilani-Dubai Campus.

COURSE PLAN :

Week 1: Review of Basic Computer Organization, Performance Evaluation Methods, Introduction to RISC Instruction Pipeline, Instruction Pipeline and Performance.

Week 2: Pipeline Hazards and Analysis, Branch Prediction, MIPS Pipeline for Multi-Cycle Operations.

Week 3: Compiler Techniques to Explore Instruction Level Parallelism, Dynamic Scheduling with Tomasulo's Algorithm and Speculative Execution.

Week 4: Advanced Pipelining and Superscalar Processors, Exploiting Data Level Parallelism: Vector and GPU Architectures, Architectural Simulation using gem5.

Week 5: Introduction to Cache Memory, Block Replacement Techniques and Write Strategy, Design Concepts in Cache Memory.

Week 6: Basic and Advanced Optimization Techniques in Cache Memory, Cache Optimization using gem5.

Week 7: Introduction to DRAM System, DRAM Controllers and Address Mapping, Secondary Storage Systems, Design Concepts in DRAM and Hard Disk.

Week 8: Tiled Chip Multicore Processors(TCMP), Routing Techniques in Network on Chip(NoC), NoC Router Microarchitecture, TCMP and NoC: Design and Analysis, Future Trends in Computer Architecture Research.