COMPUTER ORGANIZATION & ARCHITECTURE : A PEDAGOGICAL ASPECT

MULTI FACULTY

TYPE OF COURSE : Rerun | Elective | UG
COURSE DURATION : 4 weeks (18 Jan'21 - 9 Apr'21)
EXAM DATE : 24 Apr 2021

Intended Audience : UG CSE, Electrical and Electronics Engineering, Electrical Engineering and Information Technology.
Pre-requisites : Digital Design.
Industries Support : Processor design industry like Intel, AMD, etc.

COURSE OUTLINE:

Computer Organization and Architecture (COA) is a core course in the curricula of Computer Sciences as well as Electronics and Electrical Engineering disciplines at the second-year level in most of the Indian universities and technical institutions. This is the first course in COA and the course would provide students with an understanding of the design of fundamental blocks used for building a computer system and interfacing techniques of these blocks to achieve different configurations of an "entire computer system".

This course will be developed and taught with respect to Objectives based on Bloom's Taxonomy. First, we will highlight the main objectives the course is aimed to achieve. Following that, at each module, we will specify the module level objectives and demonstrate how these objectives meet the course level main goals in unison. At the leaf level i.e., the units, we will point the specific objectives of the lecture. Also, it will be demonstrated how the unit level objectives satisfy the parent module level objectives. Further, each module will have a module level problem which needs concepts of all the units therein to solve. Finally, a comprehensive course level problem related to design of "entire computer system" will be discussed which meets all the course level objectives.

ABOUT INSTRUCTOR

Dr. Santosh Biswasb is an Associate Professor in the Dept. of CSE IIT Guwahati. He has an experience of 8 years in teaching. His research interests are Fault Tolerance, VLSI Testing, Embedded Systems.

Dr. J K Deka is a Professor in the Dept. of CSE IIT Guwahati. He has an experience of more than 20 years in teaching. His research interests are Formal Modelling and Verification, CAD for VLSI and Embedded Systems (Design, Testing and Verification), Data Mining.

Dr. Arnab Sarkar is an Asst. Professor in the Dept. of CSE IIT Guwahati. He has an experience of 3 years in teaching and about 2 years in industry. His research interests Real-Time and Embedded Systems, Computer Architecture, Algorithms.

COURSE LAYOUT

Module 1: Basics: Functional Blocks in a Computer System, Number system and Computer Arithmetic (Week 1)

Module 2: Addressing Modes, Instruction Set and Instruction Execution Flow (Week 2, 3 and 4)

Module 3: Hardware and Micro-program based control Unit Design (Week 5, 6 and 7)

Module 4: Memory Architecture (Week 8, 9)

Module 5: Peripherals and Input-Output (Week 10, 11)

Module 6: Performance Enhancement of Processor (Week 12, 13)