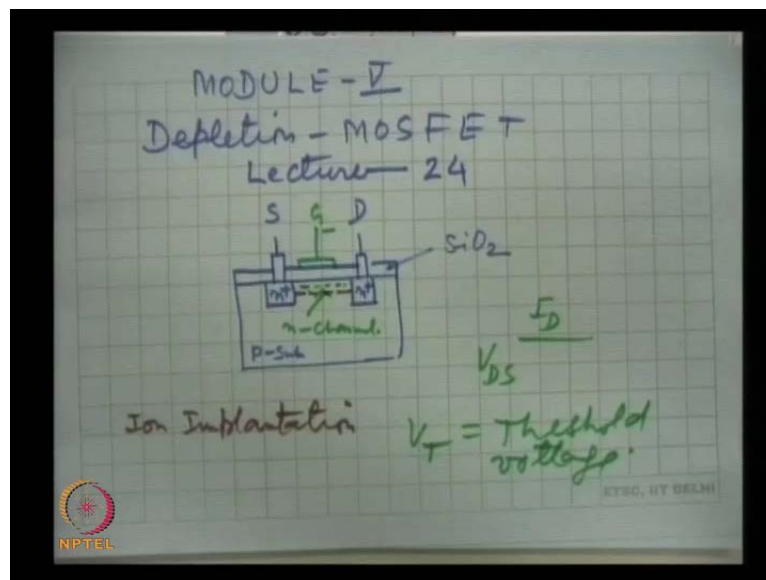


Electronics
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Module No. # 05
FETS and MOSFETS
Lecture No. # 03
Depletion – MOSFET

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We continue our discussion on the depletion MOSFET. Just to remind you that, what we have done so far that the construction of depletion MOSFET - D MOSFET was that we took a P type silicon, P substrate in which there were two heavily doped n regions, they are created by doping. And there is a oxide layer, this is the oxide layer. And by cutting by etching two windows in the oxide layer, we get the two electrodes. One is source S, and the other is drain, and here this is the SiO₂ by ion implantation a channel is created here. Ion Implantation is a very sophisticated technique by which we can dope very precisely the region where we want to dope, and how much we want to dope.

So both controls are very precise in ion implantation. **Ion implantation** is the process very modern sophisticated technique by which we can precisely dope the selected regions

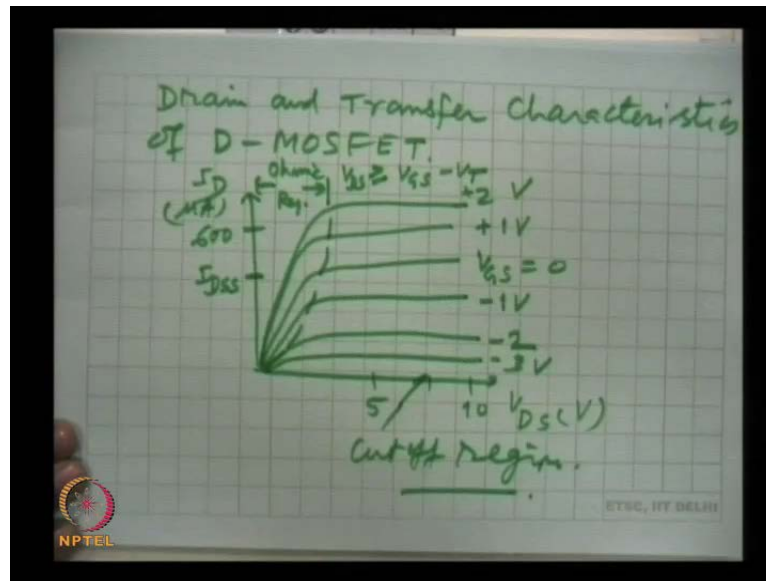
precisely. So the channel is created, and this is n channel, and then there is one electrode which is gate electrode, this was the structure. Now, here between drain and source when we establish a voltage V_{DS} , then current will flow, because there is through this channel there is continuity between source and drain. And current will be I_D the drain current will flow, and in the channel this current will be, because of the mobile electrons which have been implanted. Now, when we apply a negative voltage, then I am not repeating what we have already done that depletion region will occur and that will change the conductance of the channel.

That means the negative field, negative voltage at the gate will induce positive charges in the channel region. And these positive charge some of these positive charges will recombine with the electrons in the channel. And hence, the density of electrons in the channel will fall and there will be reduction in the conductance.

So keeping this voltage fixed at some negative voltage. And then when we plot the variation of the drain current with drain source voltage, then this current will be less. We keep on increasing the negative voltage at the gate potential with respect to source. Then more and more positive charges will induced, that means the depletion region will spread further in the channel region. And, the voltage which will take away, this is important which completely depletes the charges from the channel that is known as V_T .

V_T is the threshold voltage that gate voltage, which depletes the mobile charges from the channel completely. That is known as V_T , the threshold voltage. Now we are in a position to talk about the drain and transfer characteristics of the depletion MOSFET, which we may write as D MOSFET as well.

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So drain and transfer characteristics of D MOSFET. We talked in the previous lecture that because of the oxide layer which isolates the gate electrode from the semi conductor. We can apply in the depletion MOSFET, we can apply a negative voltage, zero voltage and a positive voltage. When we apply the positive voltage to the gate then it will induce charges in the negative charges in the channel region. And hence, the conductance will increase and it will keep on increasing when we increase the positive gate voltage further.

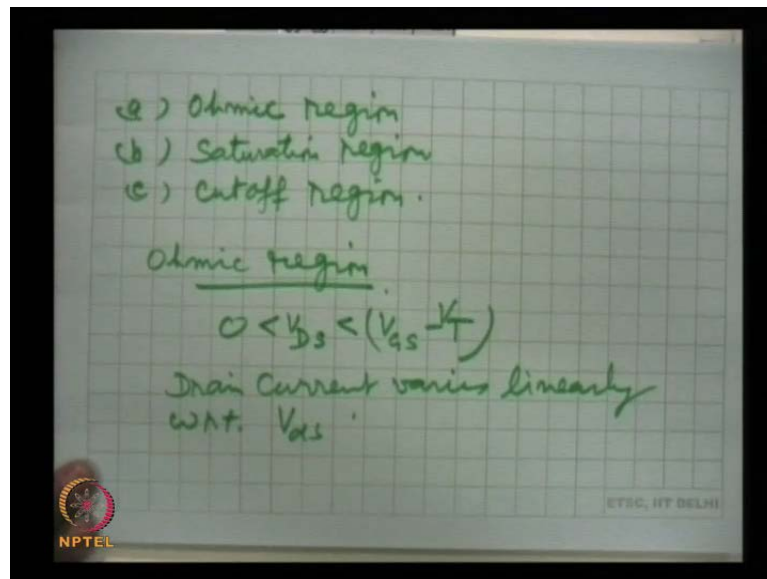
So, the drain characteristics are like this. This is $V_{GS} = 0$, this is minus 1 volt, minus 2 volt and minus 3 volt and here this is plus 1 volt 2 volts. So, when the gate source voltage is 0, what is the current flowing? We still call it I_{DSS} , the drain current when gate is shorted with the source, that current we continue to call I_{DSS} .

But, unlike the junction field effect transistor, where this I_{DSS} was the maximum current in the device. This is not true in the case of the depletion MOSFET. In the depletion MOSFET the current can increase, and it does increase when we give a positive voltage to the gate electrode. So, this is drain current and this is V_{DS} this is in volts and this is in micro amperes or milli amperes. And this may be for example, somewhere here for a particular device 600 micro ampere, this may be 5 Volts 10 Volts and so on. So these are the characteristics.

Now, again the characteristics can be divided into three regions. This is the locus of the point from where a kind of pinch off occurs. And the drain current shows almost independence with the V_{DS} . Here this independence is not as high as in the case of junction field effect transistor, where these curves were very horizontal. Here there is a slight angle as I have tried to draw.

And this is the boundary and this is called Ohmic region and this boundary is where V_{DS} has to be greater or equal to V_{GS} minus V_T . V_T is the threshold voltage. And this region, this is the Saturation region. So we have Ohmic region, Saturation region and here below this is the Cut off region.

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We will discuss these 3 regions of the drain characteristics. The first is Ohmic region, second is Saturation region and the third one is Cut off region. And, we first take Ohmic region.

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Remember on the left of these dotted lines, this is the region which is called Ohmic region. And obviously in the Ohmic region, the drain current varies linearly with the V_{DS} , as we are seeing. And, V_{DS} has the value, V_{DS} is greater than 0 but less than V_{GS} minus V_T .

This is the value of V_{DS} . V_{DS} is more than; (Refer Slide Time: 05:36) this is zero point so, it has to be more than 0 but less than this and then we get the Ohmic region. And here the drain current **drain current** varies linearly with respect to V_{DS} .

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Handwritten equations on a grid background:

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

for small values of V_{DS}

$$I_D = K [2(V_{GS} - V_T)V_{DS}]$$

$$I_D \propto V_{DS}$$

$$K = \text{Constant} = \frac{I_{DSS}}{V_T^2}$$

NPTEL logo is visible in the bottom left corner of the image.

And the drain current can be shown. It is given by this expression I_D , the drain current is equal to $K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, this is the expression. And, for small values of V_{DS} which is true for this region.

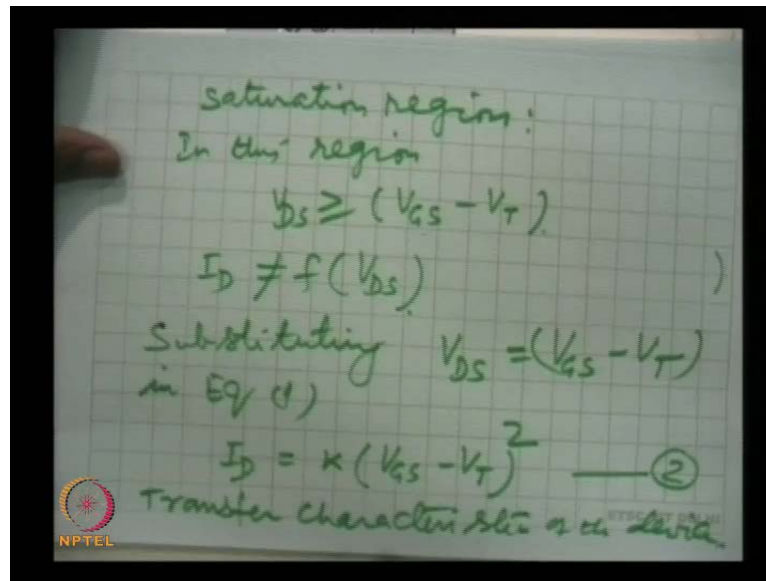
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For this Ohmic region V_{DS} is very small. So for small values of V_{DS} , these square terms can be neglected and I_D can be written as $K [2(V_{GS} - V_T)V_{DS}]$. Here this is the relation which shows that current is proportional to V_{DS} . This is what we observe here.

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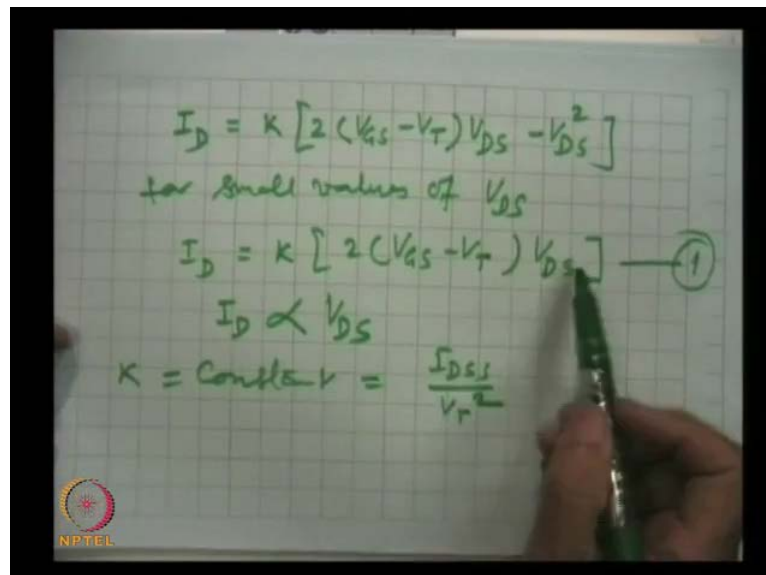
The current is dependent on V_{DS} and almost linearly it varies with V_{DS} . And K is a constant, it is a device constant and this is equal to I_{DSS} / V_T^2 . This is the constant K . So, the I_{DSS} is known for the device, V_T is known we can calculate this k and we can find out this is the relation for the drain current as a function of V_{DS} and also depends on V_{GS} . So this is how we explain the Ohmic region.

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Now, the Saturation region. This is the region and in this region V_{DS} is greater or equal to V_{GS} minus V_T . Here as the relation shows that the drain current I_D is almost independent of V_{DS} it does not depend, it depends very lightly very very little. But for the time being we may say that I_D the drain current is not a function of V_{DS} .

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Now substituting V_{DS} , this equation we call as equation 1. Then in this we can substitute V_{DS} by this quantity. So, substituting V_{DS} equal to V_{GS} minus V_T in

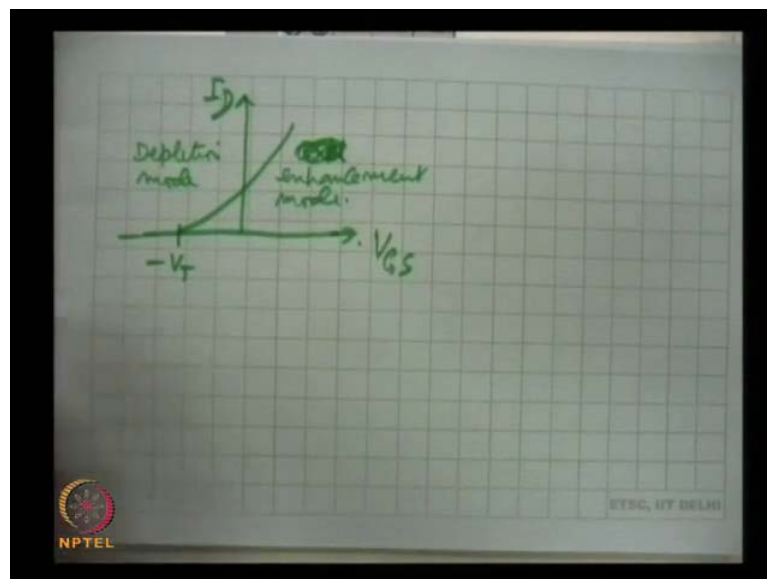
equation 1 we get I_D is K equal to $V_{GS} - V_T$ square. We call it equation 2. Now, this gives us what we are talking about; we are talking about the saturation region

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This region, on the right of this dotted line, this is the saturation region and we are saying as we are seeing here. That the drain current does not depend on the voltage between drain and source.

So this shows independence of I_D with the V_{DS} drain source voltage. But it gives a relationship between the drain current, its dependence on the gate source voltage. Now that means this equation represents transfer characteristics **transfer characteristics** of the device. We can plot I_D from this equation which is the equation of parabola, and parabolic characteristics the transfer characteristics for the device we can get. And by this equation, by taking different values of V_{GS} and I_D and the curve which we get.

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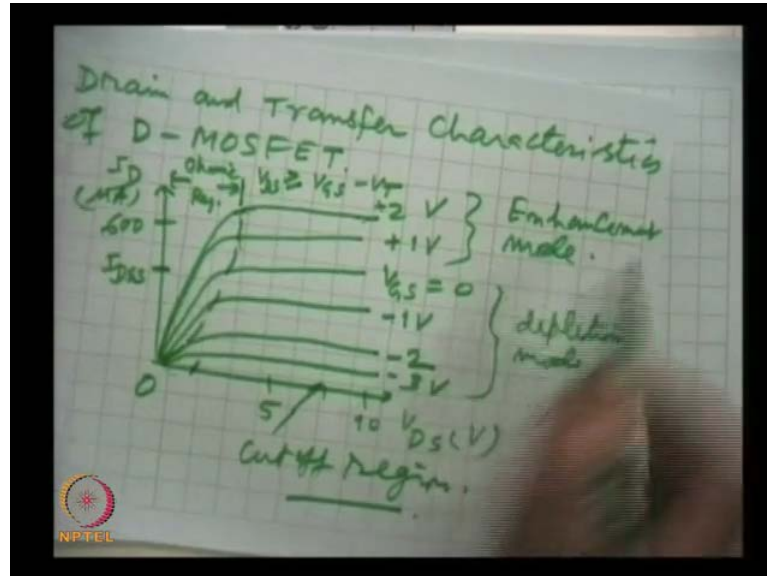


This is I_D and this is V_{GS} gate source voltage, this is the current and this is the threshold voltage which puts I_D equal to 0. And this is for the depletion mode and this part is for enhancement mode **enhancement mode**.

This is 0. Now, such a plot this is important. Such a plot can be obtained from drain characteristics also. (Refer Slide Time: 05:36) If we take different values of V_{GS} and plot the variation in I_D . So taking it has minus 1, take the corresponding I_D . V_{GS}

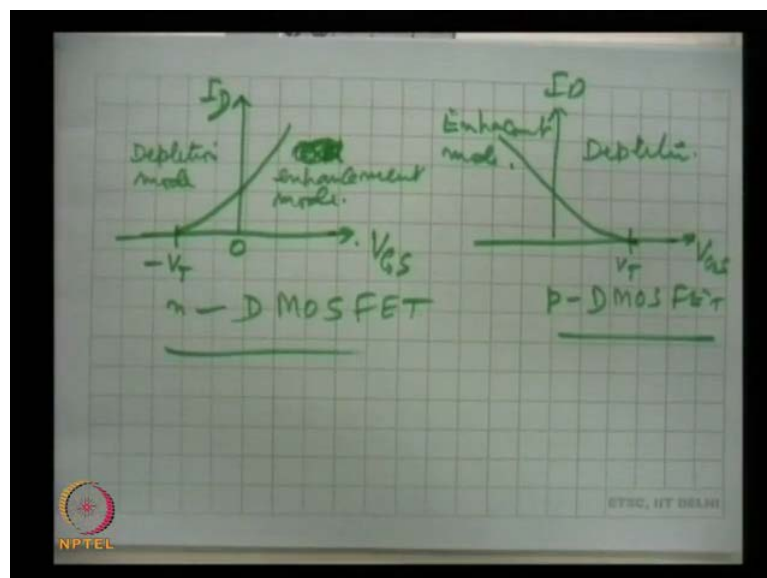
minus 2, take this value and this way we can collect all the values of V_{GS} and corresponding values of I_{DS} we can plot.

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This is the depletion mode and this is the enhancement mode. So, if we plot these points we come for this part of the plot.

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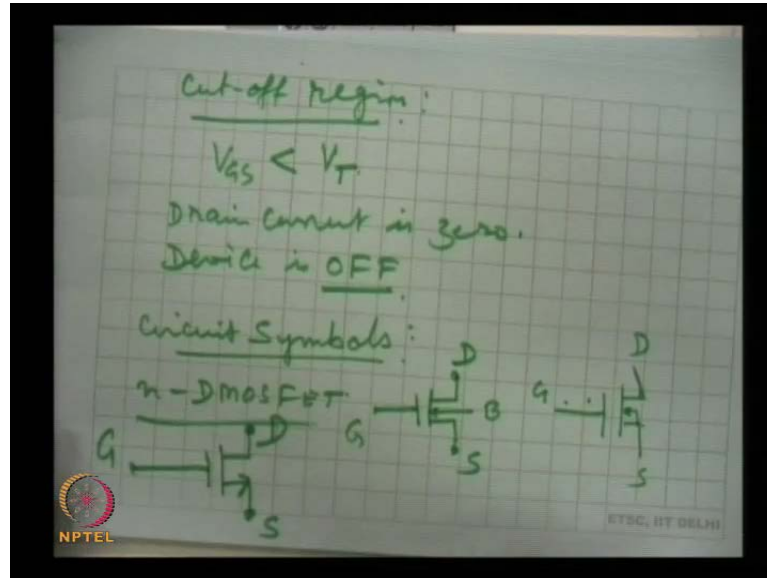


This is for n channel depletion MOSFET. For p channel MOSFET, which we call popularly as p depletion MOSFET. This plot will be like this. This is for the enhancement mode, this is for the depletion mode of the p channel depletion MOSFET.

This is I D, this is V T and this is V G S, this is the depletion and this is the enhancement.

So, this way we can get these characteristics and then the cut off region. So this is about the saturation region and then cut off region.

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In this region, the gate source voltage is less. That means, more negative than V T threshold voltage. And we have told what is the threshold voltage, that gate source voltage which depletes the charges from the channel completely.

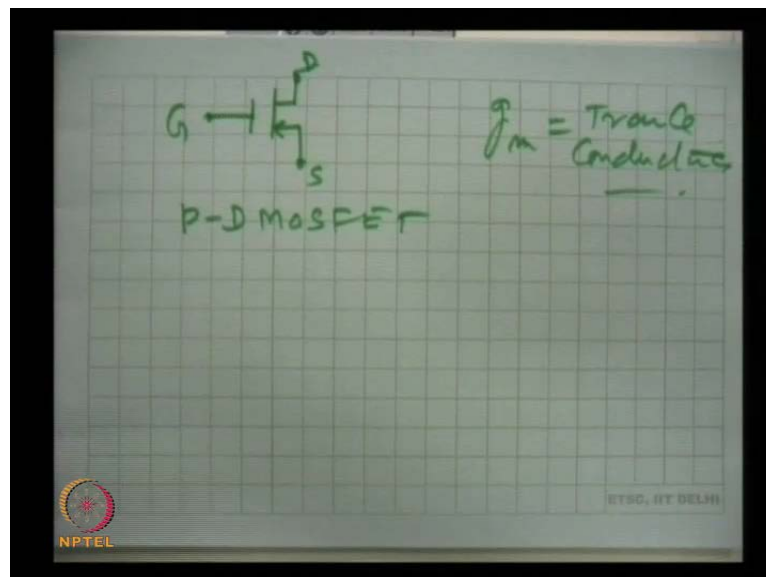
And, the drain current is zero **drain current is zero** and the device is off. These are the 3 regions of the drain characteristics of the depletion MOSFET. (Refer Slide Time: 05:36) These were the characteristics Ohmic region, Saturation region and this region is Cut off region where the device is off.

Now, about the circuit symbol for the depletion MOSFET. Circuit symbols for n channel depletion MOSFET. The one symbol is this. This is gate, this is drain, this is source and the arrow this B is the substrate. Now in many devices, in fact in most of the devices the substrate is shorted to the source. And so, this is in **in** some devices for some specific purpose which gives the more flexibility of connection like a device having 4 electrodes substrate, gate, drain and source.

But, these are only very few applications for this kind of connections. So normally with 3 electrodes the device is kept and that is here. This is drain, this is source and it is implied that it is shorted and this is gate. Now, with depletion with the junction field effect transistor note this gap.

This gap does not exist in the symbol of junction field effect transistor. This gap is the presence of the insulating layer SiO_2 layer that is depicted like this and this symbol is further simplified. So very frequently we will find this. This is the symbol most widely used. This is gate, source, drain, this is for the n MOSFET and for p MOSFET.

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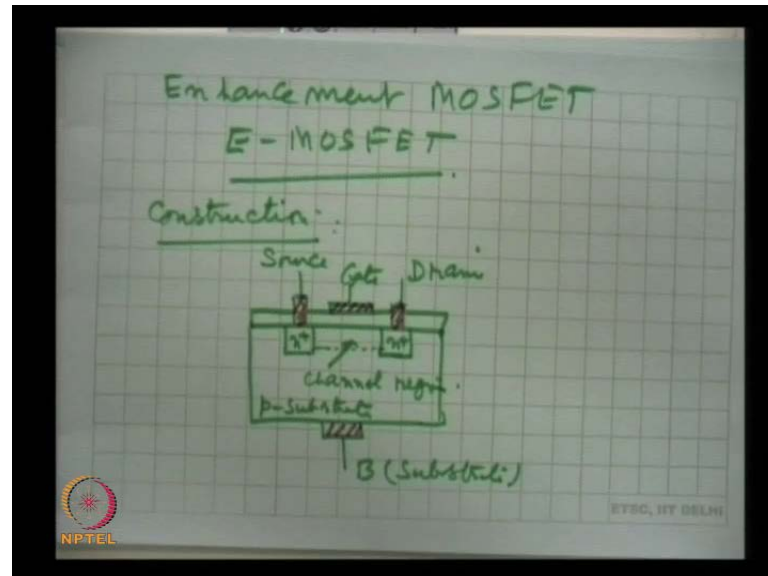
The symbol which is most widely used is this. Drain, source and this direction of arrow is reverse in the p depletion MOSFET. Gate, drain, source this is that indication of insulating layer between gate and the semi conductor. And, so this is all about the depletion MOSFET.

So, remember depletion MOSFET can be used in depletion mode and enhancement mode. And, we have talked almost about the construction, about the working principle of MOSFET. We have drawn the drain and transfer characteristics.

Transfer characteristics are very important for this device. Because here the gate voltage controls the drain current. So, the output current is changed by the gate voltage, the input voltage. So current by voltage that is g_m trans conductance. We will talk about it g_m

transconductance. Transconductance of the device will be most important parameter of a FET and MOSFETs.

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Now, we go for the next MOSFET, that is Enhancement MOSFET, which is also written as E MOSFET. First we take construction. The construction of Enhancement MOSFET is very similar to the depletion MOSFET.

But, there is a one major difference and that difference makes the whole difference in its operation, in its characteristics. And the difference is that channel does not exist at all initially. In the depletion MOSFET, you will remember that the channel was implanted, was created by the implantation.

Here there is no channel. And, when we apply a so that for example, when gate voltage is 0, then there is no continuity between the drain and source. And hence if we apply a voltage between drain and source there will not be any drain current.

So the device will be off normally which is just opposite what it was in depletion MOSFET. In the depletion MOSFET whether, there is any voltage applied to the gate or not because of the presence of the channel, there was a drain current for applied voltage between drain and source.

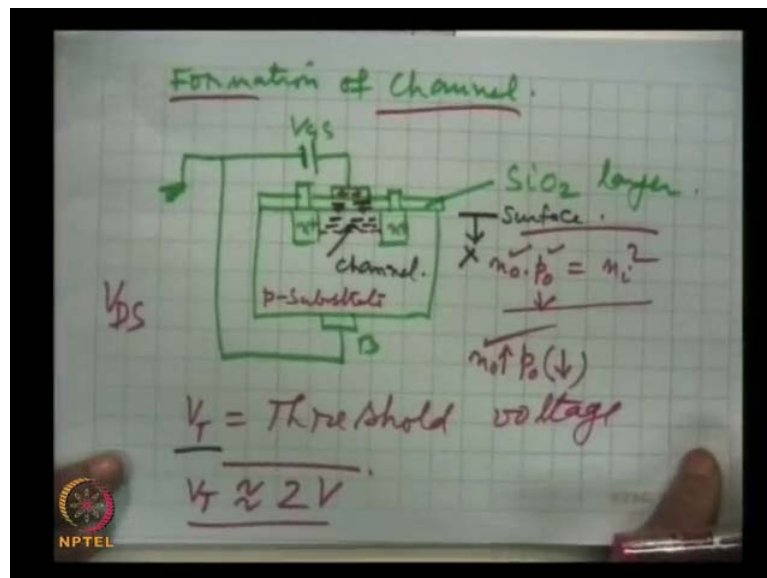
So, the construction goes like this. This is a P substrate and here 2 regions are created, heavily doped n type. And then, there is a oxide layer **oxide layer**, over that another

electrode that is gate. So, these are metallic contacts here, here and here. These are the metallic contacts and this is source, this is gate and this is drain and this is the channel region. But there is no channel, remember in enhancement MOSFET there is no channel initially, which exist in the device.

At the fabrication of time there is no channel. And so this is channel region. We will just talk how the channel will be formed; it is formed in this region. So this is channel region. And here is a substrate electrode, this is also metalized and this is B the substrate. This is the construction of enhancement MOSFET. Significant point is that, channel is not implanted and channel does not exist initially between drain and source in a enhancement MOSFET.

So obviously when we apply any voltage, because there is no connectivity between drain and source. So, no current will flow. Now, let us see what happens when we apply we will forget for the time being the voltages V_{DS} , we are not applying. We will show you that how a channel can be formed by the application of a positive voltage between source and gate.

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So, what we are talking is formation of channel. This is the device which we have talked n plus n plus electrode electrode and oxide layer. This is S i O 2 layer and here is the other electrode. Now we apply this is b, the substrate and we apply a positive voltage V G S to gate, this end is grounded and the body, the substrate is connected.

So this establishes a positive voltage. Now with the positive voltage what will happen? This is interesting and important that how a channel is formed by positive voltage at the gate terminal. The positive voltage will give rise to positive charges on the gate electrode. So, this is the voltage which is established between this semiconductor and this gate electrode.

This will polarize the surface of SiO_2 the silicon dioxide dielectric layer. So, here negative charges and positive charges will be on the two sides of the insulating layer. So what this positive charge will do?. This is a p substrate. These positive charges will repel certain holes from this channel region. Holes will be repelled by this induced positive field through SiO_2 .

So holes will be repelled and that means in this region, there will be reduction in the hole density. Because of this reduction, we know the fundamental $n_0 p_0$ is equal to n_i^2 square, fundamental relation which is true for a semiconductor. That the electron density multiplied by hole density is equal to the square of the intrinsic carrier density.

Now this hole density will fall. P_0 will fall because of the repulsion of the field created by the positive voltage at gate electrode. And hence according to this relation, if hole concentration falls, the electron concentration will go up, this will go up to maintain this constant. So, in this region some electrons will be created. I repeat how we get it? Positive voltage at the **at the** gate electrode polarizes the dielectric, and on the surface in contact with the electrode there will be negative charges.

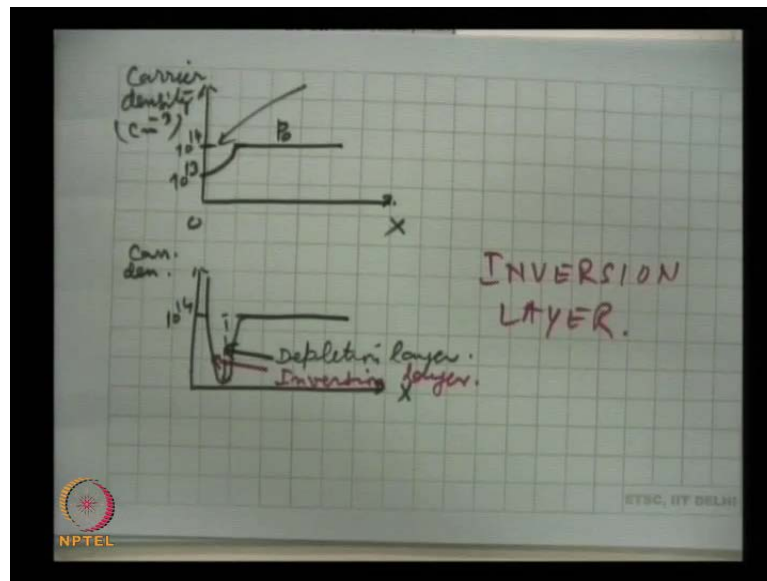
And on the opposite side which is in contact with the p substrate, the positive charges will repel holes from here. And holes repulsion implies that the electrons from the other parts of the substrates, they will rush to this region in some electrons will be there. If we further increase this voltage, then further reduction in hole and further enhancement in the channel at a certain voltage and that voltage we call as V_T , the threshold voltage. At this voltage the channel is completely formed.

So this is the channel. If you remove the voltage channel disappears. So this device is operated only at the voltages which are in axis of V_T , the threshold voltage. And for the current devices normally, V_T is of the order of around 2 volts. So, gate voltage has to be positive and it has to be more than 2 volts only then the channel will be formed. And

once the channel is formed, we apply V D S drain, source, voltage the current will flow. Because now, there is a connectivity between source and drain through the channel

So this is about the construction. Let me elaborate this point, that how initially there is a depletion region created. Because this fall in hole density is like creating a depletion. Therefore if I plot **if I plot**, this is the surface and this direction we take x, this is the surface. So, how the density in this region will vary as a function of x, that we plot here.

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This is carrier density **carrier density** that means number of charge carriers per unit volume per c c. This is x and if this concentration is p 0 in the rest of the material. (Refer Slide Time: 32:29) Here in this region the concentration here and this is we are closer, this is 0, we are closer to the surface.

So this is the depletion, this density initially in everywhere in the bulk (Refer Slide Time: 32:29) p type substrate is p_0 . And p_0 let us take as 10^{14} , the density of holes 10^{14} . But because of the repulsion of the field created at the **at the** gate will repel and this falls down by one order of magnitude say, roughly 10^{13} . On further reduction when electrons move towards that region then, what happens is this.

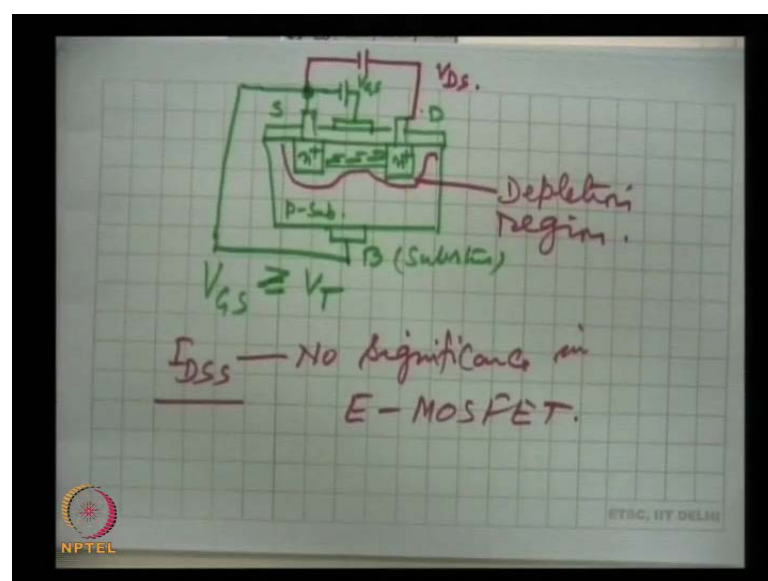
This is carrier density. This is 10^{14} as here. So this is the on further increasing the more depletion will occur. So finally, this will be the depletion layer. And this one let me draw it in the red, this one, this is the inversion layer **inversion layer**.

Why inversion? See here. (Refer Slide Time: 32:29)

This is p type substrate, there are plenty of holes. And in this p region now there is a region excess of electrons. So it is a inversion from majority hole density very important thing. Here, in the p substrate holes are in majority, electrons are in minority. But in the channel region reverse has happened.

Here the electron density has gone up by 1 or 2 orders of magnitude as compared to the electrons here. So, a channel has been created. So this is called Inversion layer. So, an Inversion layer is created and the device functions.

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Now here finally, what we have is this n plus n both are heavily doped n regions. This is p substrate p silicon normally. And here this is the channel formed, this is the other electrode and here we have applied a positive voltage. And between this is source, this is drain and one thing which is understood but we have at least in this device we have not yet talked.

That is, this is p substrate, this is n regions. So, there will be a depletion, the high resistivity region will separate this source and electrode. That means here, this is all the depletion region wherever n and p type semi conductors meet and there is structural continuity then, depletion region has to occur, it always occurs.

And what gives rise to this depletion region. The natural processes, the natural processes of diffusion and drift as we discussed in the case of p n junction formation the depletion region occurs. So same the depletion region is here. Depletion region is devoid of mobile charges and it is a high resistivity region.

So, this high resistivity region separates the active region of the device. This is the active region of the device. This is of course, the channel this is the channel. And now, we will discuss, that we can apply the voltage. But remember that V_{GS} , this V_{GS} for this channel to remain there V_{GS} very important has to be at least equal to V_T . In fact it is normally greater than that.

If, the gate source voltage is less than the threshold voltage, channel will not be formed. And so the device works only when there is a channel and for that we should remember this. And now, if we apply let me complete this circuit, this is shorted to this substrate B. If we apply a (V_{DS}) established a potential difference between drain and source. This is V_{DS} . So, maintaining the gate at a voltage larger than the threshold voltage. And now when we change, the current will be totally dependent on V_{GS} .

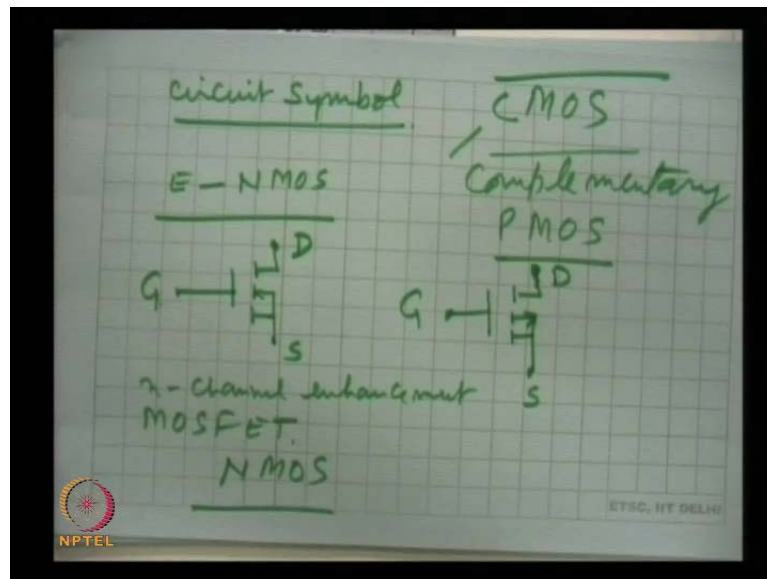
For small values of V_{GS} we will draw a soon the drain characteristics, that for different values of V_{GS} . Once the channel is formed, again this is very important parameter. Once the channel is formed, increasing gate source voltage will enhance the conductivity. I repeat, once the channel is formed and this will happen at gate source voltage in excess of threshold voltage.

And once it is formed, then further rise in the value of gate source voltage will increase the conducting electrons in the channel region. And hence it will enhance, it will increase the conductance of the channel. This way more current obviously for the same drain source voltage more current will flow. The drain current will increase.

So, let me see what I am saying once the channel is formed. Let us keep at certain voltage V_{GS} has to be positive, has to be higher than V_T and then we change we start from 0 voltage drain source voltage zero. And then we go for 1 2 3 4 5 5 volts 10 volts.

So, the current will be a function of this voltage and we will draw the characteristics that how the saturation will occur and so on. So this is about, here in this device obviously I_{DS} has no significance. No significance in E Enhancement MOSFET. Now we talk of circuit symbol Enhancement MOSFETs are shown like this circuit symbol.

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Now here what we have taken is a p substrate and we get a n channel, popularly it is known as E MOS N MOS. So, for enhancement N MOS when n type. So in brief this is written as E N MOS and the circuit symbol for this is this perforation, in this drain source this is specific to enhancement mode.

This is drain, this is source, this is gate. This is the circuit symbol for n channel Enhancement MOSFET. I said that often the n channel MOSFET it is simply written as,

it is so popular that it is said N MOS. N MOS tends for n channel enhancement MOSFET in circuit symbol is this.

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For the p type we will have to use a n substrate. Here n substrate heavily doped 2 p regions they will form source and drain and is insulating layer and then electrodes. Construction is the same except, there we will have to start with n type substrate and we will have to create p regions.

And when channel is formed that will be formed because of the inversion layer, and the inversion layer will contain the holes and the transport will occur because of holes. The circuit symbol for P MOS is perforation and then here the direction of arrow reverses. This is drain, this is gate and this is source.

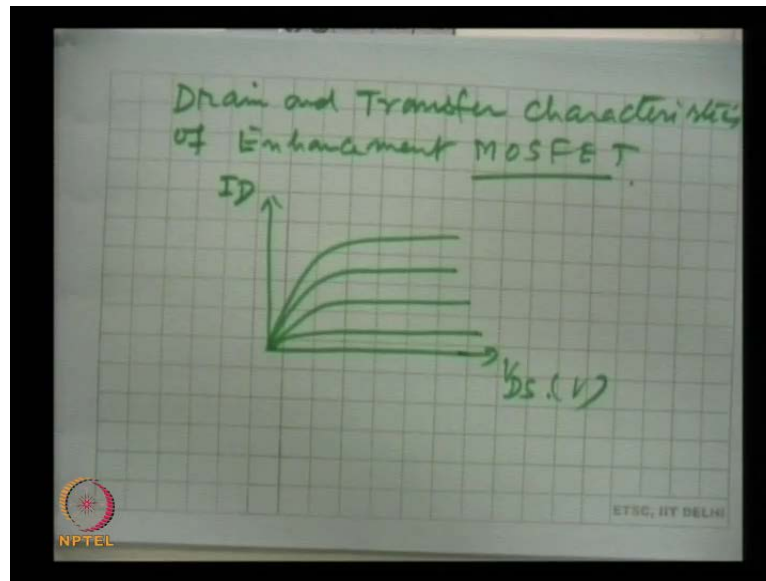
P MOS is normally having lesser use, lesser devices as compared to N MOS. But why every time I am talking N MOS and P MOS. We will talk later about the complementary devices and complementary C MOS. It is known as popularly as C MOS. C stands for Complementary.

So in the C MOS on the chip the N MOS and P MOS are simultaneously present. They are present the combination of N MOS and P MOS makes what we call C MOS, the complementary MOS device. C MOS are very very popular and till today C MOS has the least power consumption among all the MOSFETs. We will talk about that device and that is the reason because of the very little power consumption in that.

For example, a battery in our wrist watches that last for several years. So C MOS we will be talking. So C MOS in C MOS the P MOS and N MOS are simultaneously present. Otherwise, as far as amplifying device MOSFET as amplifier is concerned. Then normally N MOS will be used, we can use P MOS also but N MOS is more popular.

Then we go for i v characteristics that is drain characteristics of that device. Drain and transfer curve.

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Drain and transfer characteristics of enhancement MOSFET. These characteristics, we will draw, and like this they will be... This is drain current, this is V_{DS} in volts, and these characteristics again can be divided into three regions - the Ohmic region, the Saturation region, and the Cut off region, and that we will explain and we will see. The device is operated in the saturation region, when as an amplifier. I have said that the facts in general, which includes junction field effect transistor and particularly the MOSFETs. MOSFETs are used as a active device and as a passive device. They are connected as a resistors as capacitors and of course as amplifying devices. So, we will talk about on that.